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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,580	03/30/2004	Ofer Porat	EMC2-152PUS	3225

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RICHARD M. SHARKANSKY
PO BOX 557
MASHPEE, MA 02649

EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,580	PORAT ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The Oath filed March 30, 2004 complies with all the requirements set fort in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The contents of the filed specification are accepted.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Mayweather et al. US PG Pub no. 20020147947 A1.

As per claim 1:

Mayweather et al. teaches a system comprising: a transmitter board for transmitting a copy of signals produced in such system, the copy of such signals comprises serial data in a low byte serial link and in a high byte serial link, the signals include special characters interspersed in a pattern with the data in the low and high byte serial links (Figure 1 # 10, paragraphs [0014-0017]); a system analyzer board

comprising (Figure 1 # 12): a serializer-deserializer for receiving the transmitted serial data when the analyzer board is plugged into the transmitter board (Figure 1 # 14), and for converting the received data and the special characters interspersed in both the low and high byte serial links into corresponding data and the interspersed special characters in low byte and high byte parallel links (paragraphs [0019-0023]); and a logic for determining mismatches between the data and the interspersed pattern of special characters in the converted low byte parallel link and the converted high byte parallel link (Figure 1 # 20) and for producing a reset signal for the serializer-deserializer when a predetermined plurality of mismatches is determined (Figure 1 "RST", paragraph [0029]).

As per claim 2:

Mayweather et al. teaches the system as rejected in claim 1 above, wherein the logic maintains a count of the number of mismatches (Figure 1 # 22), such system providing a reset signal to the serializer-deserializer when a predetermined plurality of mismatches has been indicated (paragraph [0037]).

As per claim 3:

Mayweather et al. teaches a system analyzer, comprising; a transmitter board for transmitting a copy of signals being produced in a system for analysis by the system analyzer, the copy of such signals comprising serial data, each such data being in a series a low byte serial link and a high byte serial link, such signals including with the data and special characters interspersed in a pattern with the data in the low byte serial link and interspersed with the data in such high byte serial link (Figure 1 # 10,

paragraphs [0014-0017]); an analyzer board adapted for plugging into the transmitter board (Figure 1 # 12), such analyzer board comprising: a serializer-deserializer for receiving the transmitted serial data when the analyzer board is plugged into the transmitter board (Figure 1 # 14), and for converting the received data and the special characters interspersed therewith in the low byte serial link into corresponding a low byte parallel link and concurrently converting the received data and the special characters interspersed therewith in the low byte serial link into a corresponding high byte parallel link (paragraphs [0019-0023]); a system for determining whether the data and interspersed pattern of special characters in the converted low byte parallel link mismatch the data and the interspersed pattern of special characters in the converted high byte parallel link (Figure 1 # 20), a determined mismatch indicating the high byte parallel link is not aligned with the low byte parallel link, such system maintaining a count of the number of mismatches (Figure 1 # 22), such system providing a reset signal to the serializer-deserializer when a predetermined plurality of mismatches has been indicated (Figure 1 "RST", paragraph [0029]).

As per claim 4:

Mayweather et al. teaches a system analyzer, comprising; a transmitter board for transmitting a copy of signals being produced in a system for analysis by the system analyzer, the copy of such signals comprising serial data, each such data in the series having lower significant bytes thereof in a low byte serial link and having more significant bytes thereof in a high byte serial link, such signals including with the data, special characters interspersed in a pattern with the bytes of each of the data in such

low byte serial link and interspersed with the bytes of each of the data in such high byte link serial data (Figure 1 # 10, paragraphs [0014-0017]); an analyzer board adapted for plugging into the transmitter board (Figure 1 # 12), such analyzer board comprising: a serializer-deserializer for receiving the transmitted serial data when the analyzer board is plugged into the transmitter board (Figure 1 # 14), and for converting the received low significant bytes of each data and the special characters interspersed therewith in the low byte serial link into corresponding lower significant bytes in a parallel low byte link and concurrently converting the received higher significant bytes in each data and the special characters interspersed therewith in the low byte serial link into corresponding parallel higher significant bytes in a parallel high byte link (paragraphs [0019-0023]); a system for determining whether the data and pattern of special characters in the parallel low byte link matches the data and the pattern of special characters in the parallel high byte link (Figure 1 # 20), a determined match indicating the high byte parallel link is aligned with the low byte parallel link and a mismatch indicating the high byte parallel link is not aligned with the low byte parallel link, such system maintaining a count of the number of mismatches (Figure 1 # 22), such system providing a reset signal when a predetermined plurality of mismatches has been indicated (Figure 1 "RST", paragraph [0029]), and wherein the reset signal is fed to the serializer-deserializer to reset such serializer-deserializer (paragraph [0021]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Mayweather et al. US PG Pub no. 20020147947 A1.

As per claims 5-9:

Mayweather et al. substantially teaches system analyzer and a system comprising; a transmitter board for transmitting a copy of signals being produced in a system for analysis by the system analyzer, the copy of such signals comprising serial data, each such data in the series having lower significant bytes thereof in a low byte serial link and having more significant bytes thereof in a high byte serial link, such signals including with the data, special characters interspersed in a pattern with the bytes of each of the data in such low byte serial link and interspersed with the bytes of each of the data in such high byte link serial data (Figure 1 # 10, paragraphs [0014-

0017]); an analyzer board adapted for plugging into the transmitter board (Figure 1 # 12), such analyzer board comprising: a serializer-deserializer for receiving the transmitted serial data when the analyzer board is plugged into the transmitter board (Figure 1 # 14), and for converting the received low significant bytes of each data and the special characters interspersed therewith in the low byte serial link into corresponding lower significant bytes in a parallel low byte link and concurrently converting the received higher significant bytes in each data and the special characters interspersed therewith in the low byte serial link into corresponding parallel higher significant bytes in a parallel high byte link (paragraphs [0019-0023]); a system for determining whether the data and pattern of special characters in the parallel low byte link matches the data and the pattern of special characters in the parallel high byte link (Figure 1 # 20), a determined match indicating the high byte parallel link is aligned with the low byte parallel link and a mismatch indicating the high byte parallel link is not aligned with the low byte parallel link, such system maintaining a count of the number of mismatches (Figure 1 # 22), such system providing a reset signal when a predetermined plurality of mismatches has been indicated (Figure 1 "RST", paragraph [0029]), and wherein the reset signal is fed to the serializer-deserializer to reset such serializer-deserializer (paragraph [0021]).

Mayweather does not explicitly teach a plurality of memory boards and a plurality of adapter boards. However, Mayweather asserts that "it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects" (paragraph [0040]). Therefore it would have been

obvious to one of ordinary skill in the art to integrate the invention in the broader system and having multiple plurality boards and multiple adapter boards, since Mayweather et al. explains the most elemental part of the invention and to integrate it in the system there will be a need to include a plurality of basic elements. Further it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art: *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. (6983362 B1, 6742134 B1, 6374389 B1 and 5623507 A) mention the same use of SERDES to determine mismatches are included herein for Applicant's review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S.S

Saqib Siddiqui
Art Unit 2138
09/27/2006

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100